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#### **PROPOSAL SUBMITTED TO** JET PROPULSION LABORATORY

### **PROJECT TITLE:** SUPPORTING ELECTRONICS FOR HETERODYNE RECEIVER ARRAYS

**DATE SUBMITTED:** March 13, 2017 **TOTAL AMOUNT REQUESTED:** \$102,357

**Period of Performance:** 10/01/2018 – 09/30/2019

SUBMITTED BY: Arizona Board of Regents, University of Arizona Sponsored Projects Services University of Arizona P.O. Box 210158, Rm 510 Tucson, Arizona 85721-0158

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A Statement of Work for Support Electronics

"Far-Infrared Heterodyne Arrays"

This document describes the commitment of the University of Arizona (UofA) to participate in a Strategic Astrophysics Technology proposal led by Imran Mehdi of the Jet Propulsion Laboratory in response to NASA's ROSES announcement of opportunity NNH16ZDA001N-SAT, **to provide bias electronics, software and I&T support**.

### **Prepared for Principal Investigator:**

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# 1) Proposal Overview

The Jet Propulsion Laboratory, under the leadership of Imran Mehdi, is pursuing a Strategic Astrophysics Technology proposal under the NASA ROSES 2016 AO NNH16ZDA001N-SAT due March 17, 2017. The effort, outlined in Mehdi's RFP to the University of Arizona, is to improve the technological readiness of a 16-beam heterodyne receiver array using Hot Electron Bolometer (HEB) mixers and integrated LNAs, and an accompanying Local Oscillator (LO) chain. This is to follow-on JPL's successful SAT program for the development of a 16-beam LO array. The culmination of this effort is a flight-capable system that would be ready for ballooncraft, SOFIA, or a future (Explorer) mission. This SoW covers support electronics for the proposed receiver array and will leverage the University of Arizona's existing investment, infrastructure, and development of flight-level support electronics for focal plane arrays of this type.

### 2) UofA Statement of Work Overview

### 2.1 Summary

The University of Arizona will contribute to a single WBS element of JPL's proposed effort: the supporting bias electronics required to operate the mixers and integrated LNAs and the LO multipliers, one stage of which is to be operated in a closed-loop against each mixer's bias current. The UofA will also provide the control software needed to operate the array in a user friendly operable package, and finally will provide on-site integration and test (I&T) support at JPL.

The University of Arizona will deliver to the Jet Propulsion Laboratory an integrated bias electronics and software module that can simultaneously provide bias support for 16 channels each of HEB mixer bias, LNA bias, a PID-controller LO multiplier stage per channel, and up to 32-channels of DAC-driven multiplier biases. The hardware control will be provided by an integrated macrocontroller board with ethernet access, and user operation of the module will be possible via all of 1) direct commanding, 2) scripting, and 3) an interactive GUI.

The UofA understands that the front-end control of the 16-pixel 2 THz receiver system is a key hardware subsystem and will support the integration and testing of the system at JPL after delivery. University of Arizona key personnel will be available to participate in telecom with JPL as needed.

This subcontract will be performed on a cost-reimbursable basis and that the I&T support effort of the electronics at JPL (post-delivery) are on a time and materials basis.

### 2.2 Key Dates and Milestones

The UofA schedule (Table 1) has been focused on a primary period of performance in the Year 2 of the JPL effort, during FY19 (October 2018-September 2019). This optimization minimizes technical risk and cost and will ensure timely delivery before the required delivery date as per the JPL master schedule. Moreover the schedule proposed contributes to reduce the overall project risk by providing to JPL in FY18 a finalized design with all mechanical, electrical, and software interfaces defined. This will ensure that possible design issues that could cause significant project schedule delays are found well before starting the receiver integration in Year 2.



Project Milestone or Review	Date
Beginning of Project	10/1/2017
Selection of Electronics Technical Approach	10/1/2017
Draft of Electronics and Software Module Design to JPL	12/1/2017
Project Design Review at JPL	3/1/2018
All (mechanical/electrical/software) interfaces frozen	6/1/2018
Beginning of UofA effort, delivery of final design documents	10/1/2018
Delivery of GSE components to JPL with draft documentation	3/29/2019
Initial on-site support of GSE elements at JPL completed	4/30/2019
Final documentation delivered to JPL	4/30/2019
Project ends	9/30/2020

Table 1: UofA Key Dates

# 3) UofA Work Commitment Description

# 3.1 Major deliverables

The University of Arizona will provide the Ground Support Equipment (GSE) components, with subcomponents listed in Table 2. The system will be delivered with complete operational documentation, software and corresponding test data. JPL will provide to the UofA prior to the 3/1/2018 review any changes to the nominal mechanical, electrical, and software interfaces so that the design can then be frozen. The UofA GSE equipment shall be similar to STO-2 or GUSTO flight electronics and in compliance with JPL's specification for safe operation of the 16-pixel HEB array and corresponding LO units.

Iten	n	Qty	Туре	Delivery Date	JPL WBS#
#1	Bias Electronics Module	1	GSE	3/29/2019	TBD
#2	Bias Electronics Software	1	GSE	3/29/2019	TBD

Table 2: List of Major Deliverables

The University of Arizona will complete delivery of the GSE by 3/29/2018. This includes 1 month of schedule reserve.

The cost of the UofA provided GSE includes the procurement of required commercial parts, fabrication of existing electronics sub-module boards and their population and testing, and integrated testing as a module to ensure compliance with project requirements.

# 3.2 UofA provided I&T Support

In addition to the effort required to produce and test the components listed above, the SoW also includes post-delivery support to ensure proper and safe integration of the delivered components into the higher level of assembly. The UofA will provide on-site technical support during this integration and remote support at other times. The UofA will send at least one qualified engineer

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for technical support during the integration of this system for end-to-end testing, optimization of the 16-beam receiver, and calibration involving the use of this GSE system. The specific commitment and tentative dates are summarized in Table 3.

Item	Start date	Commitment	JPL WBS#
#3 UofA Support for initial integration and test at JPL	4/2/2018	1 week, 1 engineer	TBD
#4 UofA support for lab measurements at JPL	9/2018	1 week, 1 engineer	TBD

Table 3: UofA Technical Support for JPL activities

### 3.3 UofA Support for Design Reviews

The UofA will support JPL under this project to prepare for internal equivalents of the Preliminary and Critical Design Reviews. At a minimum, this documentation will consist of the following:

- SAT-appropriate Technical Data Package of the Preliminary and Final Designs
- An abbreviated Development Plan including a schedule for the Work
- A draft Acceptance Test Plan with abbreviated supporting error analysis.

# 4) Technical Approach and Specifications

### 4.1 Overall requirements

The overarching requirements for the 16-beam 2 THz receiver system are shown in Table 4. Tentative mechanical and electrical interfaces are also listed.

Specification	Value
HEB bias quantity	16 channels
HEB Bias type	4-5 wire
HEB Bias range	-20 to 20 mV on device
Assumed HEB voltage divider	~100:1 (0.1V in, ~1 mV on device)
Noise on device	<1uV rms at device, <10 uV rms on monitor
LNA bias quantity	16 lines
LNA bias range	0-2.5V at up to 25 mA
Noise on LNA bias line	<1 mV rms at device
LO multiplier PID	1 per HEB, slaved to analog mixer current monitor, voltage range TBD, ~1 mA drive
Number of non-PID LO biases	32 available, more possible
Non-PID multiplier bias range	Nominal -15V to +15V at 1mA or 10mA drive, <5 mV rms
Preamplifier stage for monitors	Isense and Vsense for each of 16 mixers, gain ~100
Input Bus Power	18-36 VDC internal bus, 110 VAC 1-phase also supported

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Specification	Value
Power consumption	<75W, CBE is 4W/channel for STOarch , 1W/ch GUSTO
Mass / Architecture	<15 kg, either 3U (GUSTO) or 6U (STO) architecture
Communications interface	1 Gbps Ethernet, network server interface Internal digital interface is SPI, 'sidecar' interface is RS232
Software interface	Client-server (direct commanding, scripting, and GUI)
Mechanical interface	Installs directly onto cryostat using hermetic connectors or uses interface cables to cryostat (TBD by design review)

Table 4: Specification table for the bias electronics module.

# 4.2 Technical Approach 1: Using current STO-2 designs

The nominal technical approach assuming no other funding source is to provide an integrated electronics module that combines numerous existing electronics board designs. This follows the flight electronics modules provided for the 2017 STO-2 flight and would essentially be a repackaging of that design for laboratory use. The components to be provided within a single chassis would be:

- a) Supercam 8-channel SIS/HEB + magnet + LNA bias, quantity 2
- b) 8-channel STO-2 PID card, quantity 2
- c) 8-channel Supercam preamp board, quantity 2 OR STO-2 4-channel preamp, quantity 4
- d) Embedded control computer module from HEAT project, quantity 1
- e) Housekeeping & add-on analog multiplexer board x1
- f) Multichannel DAC board w/ drivers for non-PID multiplier biases
- g) Fixed DC power supplies from HEAT project
- h) Standalone AC to DC power supply for lab use.

The nominal height of this electronics module would be 6U and is set by the size of the standard bias electronics card and preamp board. A standard 19" rackmount interface would be provided but the module stands alone and in a smaller footprint than the 84HP wide standard indicates.

An interface that directly mounts this electronics box to the test cryostat is available and encouraged. The hermetic interface will be assigned by the time of the initial design review.

CBE mass is expected to be about 12 kg assuming DC power input and the CBE power consumption not exceeding 50W DC for a 16-channel system.

# 4.3 Technical Approach 2: Using the next-gen GUSTO design

If the GUSTO flight program is funded at least through PDR, a next-generation electronics module design will be available to provide to JPL on the same timescale. This proto-flight system is more integrated, lower power, and smaller footprint. The subsystems to be integrated would be:

a) 8-channel integrated mixer/multiplier bias board (MMBB), quantity 2

b) Macrocontroller (computer) board (CPUB), quantity 1



- c) System backplane with power supplies on back, quantity 1
- d) Optional housekeeping board, quantity 1

The nominal height of this electronics module would be 3U. A standard 19" rackmount interface would be provided but the module can stand alone and in a far smaller footprint than the 84HP wide standard indicates.

An interface that directly mounts this electronics box to the test cryostat is available and encouraged. The hermetic interface will be assigned by the time of the initial design review.

CBE mass is expected to be about 7 kg assuming DC power input and the CBE power consumption not exceeding 24W DC for a 16-channel system.

# 4.4 Key Decision Point for selection of Technical Approach

The selection decision for GUSTO will be made by the end of March 2017, so that the technical approach will be known long before the start date of the proposed effort. The KDP for technical approach will therefore be the start date of the overall effort, 10/1/2017.



# 5) UofA Budget

### 5.1 Basis of estimate

The UofA effort has been costed using a grassroots methodology, based on actual fabrication and integration costs of the components to be delivered to JPL. For Technical Approach #1, these costs come directly from the HEAT project, Supercam, and STO-2. The driving labor cost is the integration and testing efforts needed to take these disparate components and integrate them into a unified and coherent platform. For Technical Approach #2, all NRE is subsumed by the GUSTO flight electronics development plan, and the main effort is to snapshot the electronics platform at the time of the GUSTO CDR (5/2018) and deliver a cloned system to JPL for the purposes of this program. The labor and fabrication costs are similar for both technical approaches.

This subcontract will be performed on a cost-reimbursable basis.

# 5.2 Financial and workforce assumptions

Costing is based on similarity to actual hardware that has been built for STO-2 or will be built for GUSTO. This matches previously built systems built either under previously-funded NASA APRA suborbital programs or for the GUSTO Explorer Mission of Opportunity. No significant NRE or architecture changes are necessary. One month of systems-level engineering and documentation, three months of fabrication, integration and testing, and one month of software integration and testing are nominally budgeted above known fabrication and acquisition costs. One month of funded schedule reserve is allotted for the nominal 6 month build time. Travel costs are commensurate with allowable reimbursements for 1 engineer over the 1 week initial I&T in 4/2018 and 1 week final laboratory measurements in 2019. That is, I&T support effort of the electronics at JPL (post-delivery) are on a time and materials basis. A UofA standard indirect cost rate of 53.5% effective 7/2016 is applied to the MTDC base and UofA standard labor ERE rates are assumed.

Federal Fiscal Year	UofA cost quote
2019 (Oct 2018-Sept 2019)	\$102,357

# Subcontract for Electronics Module to JPL (NASA ROSES/SAT

proposal)

Organization Arizona Board of Regents, University of Arizona

PI Craig Kulesa

Originating Sponsor NASA

Overall Performance Period 10/1/2017-9/30/2020

University of Arizona Contract Period 10/1/2018-9/30/2019

Chiversity of Alizona Contract		YEAR 1		Oct 2018 to Sept 2019
	Year 1	Labor		TOTAL
	Rate	Hrs.		YEAR 1
PERSONNEL				
Senior Personnel				
PI/System & SW Engineering, PM, Craig Kulesa, 2 mo	\$ 28.08		348	\$ 9,7
Electrical Engineer, Reuben "Bud" Hill, 1 mo	\$ 45.74		174	\$ 7,9
PID board integration, Abram Young, 1 mo	\$ 35.66		174	\$ 6,20
Mechanical Engineering (integration), 1 mo	\$ 35.20		174	\$ 6,12
Senior Personnel Sub	ototal		870	\$ 30,00
Classified Staff Subtotal				
Electrical Technician, 8 weeks	\$ 23.95		320	\$ 7,6
Classified Staff Sub	ototal		320	\$ 7,60
Labor Sub	total		1,190	\$ 37,72
FRINGE BENEFITS - Rates effective 7/1/16 and beyond				
Faculty and Appointed Personnel @ 34.9%	<b>_</b> \$		30,061	\$ 10,49
Classified Staff @ 34.9%	\$		7,664	\$ 2,6
Fringe Benefits Sub	total			\$ 13,16
	-			
Personnel Labor + ERE Totals				\$ 50,89
				¢ 00,0,
OTHER DIRECT COSTS	\$-\$		-	\$
OPERATIONS				\$ 13,19
Materials and Supplies				\$ 12,50
Communications				\$ 20
Publication costs				\$
Shipping				\$ 49
TRAVEL				\$ 2,60
		Domestic		Intern'l
Pasadena, CA: 2 trips x 1 week x 1 person		Domestic		Intern
Travel to Pasadena CA: 2 trips at \$250 ea			500	
Lodging plus per diem: \$150/day x 14 days total				
	or trip		2100 2600	
Total Other Direct Costs			2000	\$ 15,79
				φ I3,/ <b>9</b>
TOTAL DIRECT COSTS				\$ 66,68
INDIRECT COSTS - 53.5%, effective 7/1/16				
MTDC BASE = Total Direct Costs (TDC) less capital equipment, less Tuition Rem	ission, and on first \$25K o	f EACH subcontract		
		MTDC Base		IDC
Base (on salaries, operations, t	ravel) \$		66,682	
Base (on first \$25K of <b>EACH</b> subcor			-	
Total Indirect Costs	Ψ			\$ 35,67
TOTAL UA PROJECT COSTS				\$ 102,35

# **University of Arizona Cost Proposal**

# **BUDGET DETAILS**

This Budget Element explains the total cost the University of Arizona (UA) is expected to incur during the period of performance of this subcontract (October 1, 2018 – September 30, 2019). The estimates include all labor costs, research materials & services, subcontracts, travel, and indirect (F&A) charges. The contract is expected to be performed on a cost-reimbursable basis.

# **DIRECT LABOR**

### Summary

The labor hours applied to the research in the period specified is 1190 labor hours. This is 0.57 FTE for the 1-year period of performance (based on 2088 hr/work year).

# **Table B1: Proposed Work Effort**

Table of Proposed Work Effort		
Name	Effort	
PI, System & SW Engineering, PM: Craig Kulesa	16%	
Electrical Engineer: Reuben "Bud" Hill	8%	
Systems engineering: Abram Young	8%	
Mechanical Engineering: Ruben Dominguez	8%	
Electrical Technician: TBN	15%	

# **Personnel**

**Craig Kulesa, PI (SE and SWE)** is an Associate Astronomer at the Steward Observatory. Kulesa will contribute 348 hours to this project support at unburdened direct labor rate of \$28.08 per hour. He will manage the overall technical effort, coordinate efforts between personnel, provide software development and integration support.

**Reuben "Bud" Hill (EE)** is a senior Electrical Engineer in the Steward Observatory. Hill will contribute 174 hrs to this project at unburdened direct labor rate of \$45.74 per hour. He will support the schematic development of refurbished preamplifier boards and PID boards.

**Abram Young (SE)** is a Specialist, Technical/Research at Steward Observatory. Young will contribute 174 hours to this project at unburdened direct labor rate of \$35.66 in support of the PID board development.

Ruben Dominguez (Mechanical Engineer) is currently a senior mechanical engineer at the

University of Arizona. Dominguez will contribute 174 hours to this project, providing mechanical integration help with the box design and mechanical support of the various boards in the electronics module at the unburdened direct labor rate of \$35.20 per hour.

**TBD** (Electrical Technician): A technician in the ETS group at Steward Observatory will work over 8 weeks of the proposal period assisting with cable manufacture, board population and enclosure construction. 320 hours of effort are budgeted at the unburdened direct labor rate of \$23.95 per hour.

### **UA Academic and Summer Terms**

The Faculty and Student employee year is broken into the academic and the summer terms. The academic term is 9 months, or 40 weeks in duration. The summer term is 3 months or 12 weeks in duration.

### UA Faculty and Student Academic and Summer Hours and Rates

Faculty members are allowed a total of 464 hours of compensation during the summer term and 1600 hours during the Academic term. The faculty summer rate is calculated using 155 hours per month. The faculty hourly rate is calculated using the following formula: Rate = (Academic Salary)\*.00072.

Graduate students are allowed to work a total of 800 hours (89 hrs/month) during the academic term and 414 hours during the summer term.

# **UA Appointed Personnel and Classified Staff Hours**

Appointed and Classified staff hourly rates are calculated using a 2088-hour work year or approximately a 174-hour work month.

### **UA Project Management Support for this Project**

The project management effort will include basic financial tracking as well as project requirements and goal tracking. The effort for these duties is over and above the typical departmental duties provided.

### **FRINGE BENEFITS**

The benefits rates are listed in Table B2. The dollar value is calculated by multiplying the benefits rate to the wages earnings for the specified period.

 Table B2: Benefits Schedule

Employee Type	July 2016 and beyond	
Full Benefits Personnel	34.90%	\$13,365
Graduate Students	13.40%	\$0
Undergrad Student	1.70%	\$0

Benefits \$ = Hours x Hourly Rate x Benefit rate

# **INDIRECT COSTS**

University indirect costs (Facilities & Administrative) apply to the subtotal of: 1) Direct Labor (including benefits); 2) Travel; 3) Supplies and materials (including equipment items costing under \$5000). The University of Arizona defines capital equipment as equipment items costing \$5000 or above.

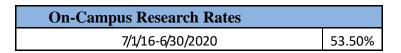
Indirect cost rates are also only applied to the first \$25,000 of each subcontract

Indirect cost excludes Graduate Student tuition and fees that are direct charged to the grant.

### Indirect Cost Rates

The following table describes the University's indirect rates for the period of performance of this proposal.

# Table B3: UA Indirect Cost Schedule:



# TRAVEL

Domestic travel to and from Pasadena, CA for one person (two trips of 1 week duration each) to support integration and test of the delivered system at JPL is budgeted.

The cost estimate for this supporting travel is described in detail in Table B4.

### **Table B4: Travel**

Travel Item	Value
Destination	Pasadena, CA
Lodging	1 person x 7 days x 2 trips = \$150 x 7 x 2 = 2100
Air/Ground Fare	\$250 x 2 = \$500
Totals	\$1300 per trip = \$2600 total

# **Subcontracts**

No Subcontracts are requested for this project.

# **CONSULTANTS**

No consultants are requested for this project.

# SUPPLIES, MATERIALS, & OPERATIONS

We request funding for research supplies (**\$12,500**) and work-flow/data capture and expenses required for the conduction of this investigation inclusive of the material costs of creating, replicating, backing up (archiving), distributing and presenting all project related documentation, memoranda, technical reports, analysis, summaries, etc. directly related to this project. The breakdown Materials and Supplies is provided in Table B5 below. We request funding for communications (**\$200**) to support bimonthly audio and video teleconferencing between all partners (principally JPL and UofA). We request funding for shipping (**\$491**) required for the conduction of this investigation inclusive of the material costs of creating, replicating, backing up (archiving), distributing and presenting all project related documentation, memoranda, technical reports, analysis, summaries, etc. All supplies described in this budget are charged at the indirect rates.

# Table B5: Materials and Supplies cost breakdown

Item	Estimated cost (vendor)
8-channel PID board prototype (2 revisions)	\$1200 (Sierra Proto Express)
8-channel preamplifier board (2 revisions)	\$1800 (Sierra Proto Express)
8-channel SIS Bias Card, fab+parts (x4)	\$3300 (Hughes or Sierra Proto)
Machining of aluminum lids for SIS cards (8)	\$1750 (URIC)
Embedded control computer module + spare	\$400 (Technologic Systems)
DC/DC converter boards (10) and parts	\$2400 (Sierra Proto, Digikey)
AC/DC supply for lab use (2)	\$250
LO Multiplier driver board (2 revisions) + parts	\$1400 (Sierra Proto, Digikey)
TOTAL	\$12,500

# EOUIPMENT

This work relies on the use of existing facilities at the University of Arizona.

### **OTHER DIRECT COSTS**

None.

# **FEE/PROFIT**

The University of Arizona has no fee/profit costs in this proposal.

### **Prepared by:**

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