CLOCK DRIVER BOARD

The clock driver board translates digital timing signals into analog waveforms whose high and low voltages can be individually programmed for direct connection to CCD and infrared arrays. It outputs 24 analog signals to the sensor. Two flavors of clock driver board are available - one for CCD arrays and one for IR arrays. They are almost identical, differing only in the placement of a capacitor on the operational amplifiers that finally drive the clock signals and in the choice of the op amp. Both boards are discussed in this document, and the differences are highlighted.

SPECIFICATIONS

Power dissipation	304 mA at 5 volts digital	10 watts total
	247 mA at +16.5 volts analog	
	258 mA at -16.5 volts analog	
Board Size	3.96 x 9.0 inches (3U width)	
Number of channels	24 output channels available on a single male DB-37 connector	
	12 outputs may be changed in a single timing board instruction	
Voltage output	+/- 10 volts maximum. Smaller ranges are selectable either by changing jumper settings or changing one voltage reference resistor.	
	60 mA sustainable current drive capability	
Rise and fall times	20 nanosec for a 10 volt change (CCD board)	
	200 nanosec for a 4 volt change (IR board)	
Resolution	The high and low rails of the clock voltages are set with 12 bit DACs, giving approximately 10 millivolts resolution.	
Diagnostic output	Any two clock driver outputs may be software selected for viewing via a pair of SMB connectors next to the DB-37 output connector.	

THEORY OF OPERATION

Fig. 1 shows a block diagram of one of the twenty-four clock driver channels. The DIN-96 connector on the left in inserted in the controller backplane to connect to power, ground and digital signals. A 37-pin DB male connector passes the analog clocking signals from the right of the board to the array.

The upper and lower voltage rails of each of the 24 clock drivers is independently controlled by two outputs of a four output, 12-bit DAC, Analog Devices DAC8420. The two voltage outputs are routed to an analog switch that selects one of the inputs. The switch output is connected to an op amp with a non-inverting gain of x2. It is an Analog Devices AD810 for CCD clock driver boards, which was selected for its fast slew rate (resulting in 20 nanosec rise and fall times for a typical 10 volts change), good drive current (60 mA sustained), and low noise. A capacitor is placed on its input to reduce over-and under-shoot at the expense of slewing rate, though about a volt of over- and under-shoot persists. For IR clock driver boards the AD829 part was selected because its slew rate can be controlled to reduce the over- and under-shoot to about a tenth of a volt, which slows down the rise and fall times to 200 nanosec for a typical 4 volts swing. A CMOS switch is placed after the op amp to disconnect the clock driver output from the array whenever the ENCK is not true. This line, controlled by the timing board, is held not true before analog power up, whenever the input power deviates from its allowed voltage range or there is a reset of the timing board DSP.

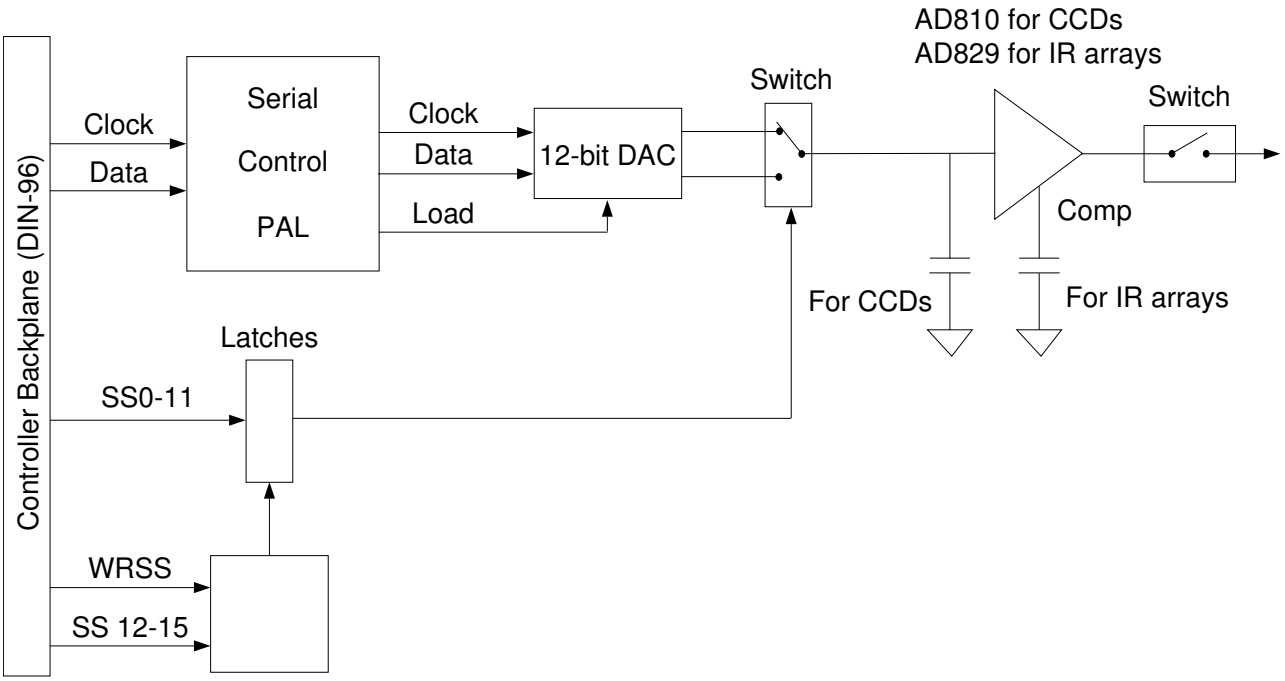

Fig. 1: Block diagram of one channel of the clock driver board

There is a provision for connecting either zener protection diodes or capacitors from each output to ground. Zener protection diodes are routinely installed on IR boards since bipolar voltages often cause latchup on their CMOS readout circuitry. The user can install capacitors on CCD boards that act in concert with the 30 ohm series resistance of the CMOS protection switches to provide some waveshaping of the output clocking signals. Small values of a few tenths of a picofarad can be used for serial clocks to improve dampen their rise and fall times, while large values of a fraction of a microfarad can be used for parallel clocks to limit the onrush of current into the CCD.

Control of the switch of each of the 24 clock drivers is derived from a set of latches that is controlled by the Switch State bits SS15 to SS0 generated by the timing board. The timing board writes its DSP data bits D15 to D0 to the backplane as SS15 to SS0 whenever the DSP writes to the memory mapped address WRSS = $FFB0, with the data bits D23 to D16 being used as inputs to the timng board delay counter and the strobe signal WRSS being asserted. The addressing lines SS15-SS12 are input to the PAL U70 to act as board and bank select lines. The data lines SS11 to SS0 are latched when the strobe signal WRSS is asserted if the address lines SS15-SS13 match the state of the board address jumpers JP8-JP5. These are marked as the three Switch jumpers 1 to 3 in silk screen on the board. The address line SS12 selects to update either the lower bank of the clock driver lines CLK11 to CLK0 (SS12 = 0) or the high bank CLK23 to CLK12 (SS12 = 1), allowing only twelve of the twenty-four clock signals to be changed in a single timing board instruction. Alternatively, the control line TIM-D-AUX can be set high to cause the lower and upper clock driver banks to update simultaneously to the same values on a single instruction, which may be useful for controlling mosaics that require twelve or fewer clocks per CCD. This is implemented in software as

```
DUALCLK         EQU         1                   ; Bit for updating both clock driver banks
        BSET    #DUALCLK,X:<LATCH               ; Change the software LATCH bit
        MOVEP   X:LATCH,Y:WRLATCH               ; Write the software value to the hardware
```

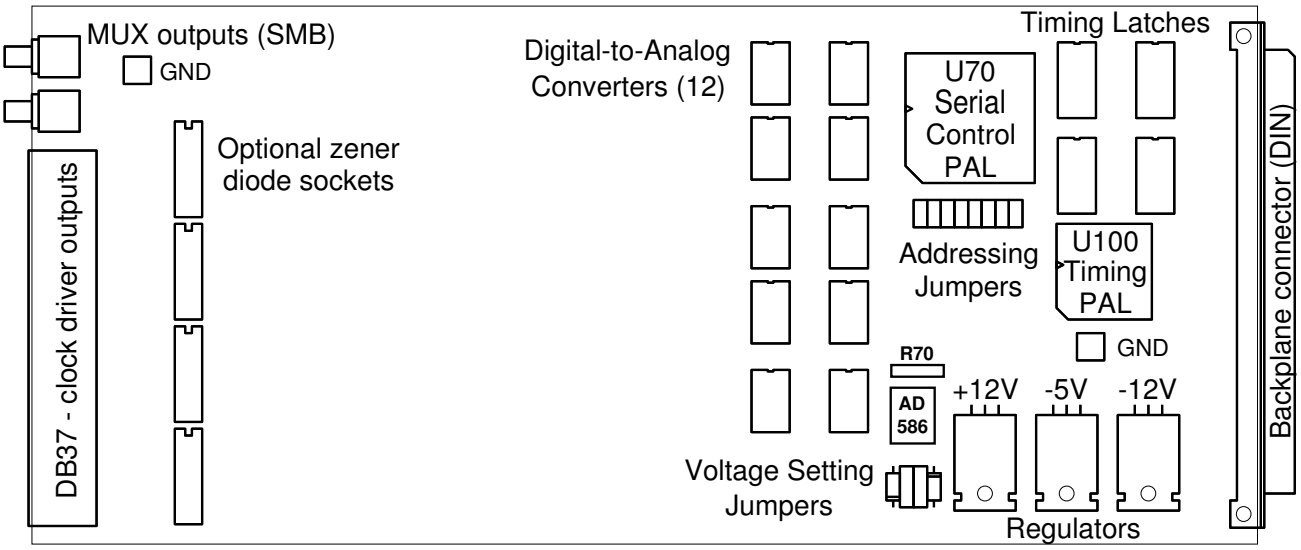

Fig. 2: Parts layout for the clock driver board.

There is a provision for the user to conveniently display two selected clock driver outputs on an oscilloscope through the two SMB (push-on) coaxial connectors mounted next to the DB-37 output connector. They are connected to a set of multiplexers (U73, U76, U77, U79-U81) that sample the clock driver outputs at the output connectors. Selection of any two outputs is made from the timing board with the command -

SMX #clk_board #MUX1 #MUX2 - "Set MultipleXer".

#clk_board = 0 to 15 to select the desired clock driver board

#MUX1 = 0 to 23 to select which clock driver output gets connected to the first SMB connector.

#MUX2 = 0 to 23 to select which clock driver output gets connected to the second SMB connector.

JUMPERS

Fig. 2 shows the location of the principal components on the board. Addressing jumpers are located beneath the socketed PAL to the right of the board, and voltage selection jumpers are located to the left of the bank of three regulators. Fig. 3 shows an enlargement of the jumper blocks.

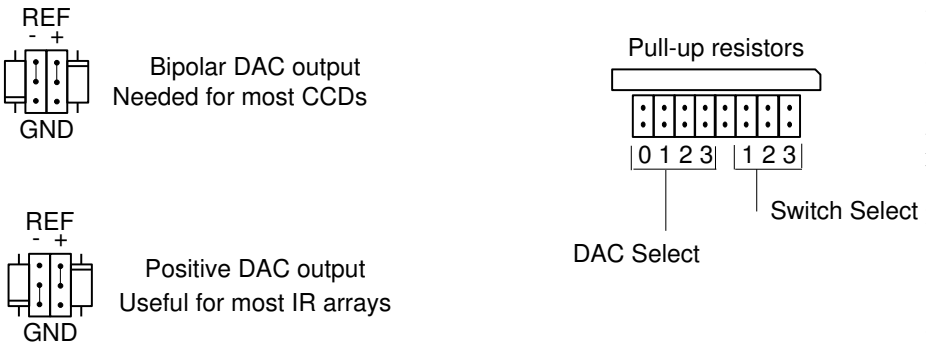

Fig. 3 - Jumper block diagrams

Voltage selection jumpers can be set to make the clock drivers either unipolar positive, unipolar negative or bipolar. Shown are settings for bipolar operation used for CCDs where both the + and - sides of the jumper block connect to the REF supply, indicating that both the high and low clock levels are con-

nected to a reference supply. Unipolar operation with positive voltage outputs is indicated below it, where the jumper marked - is connected to GND to indicate that the low clock level is set to ground so only positive voltages will be routed to the clock driver output pins.

The maximum and minimum values attainable at the clock driver output pins are determined by the value of the resistor R70, located just above the AD586 voltage reference above the voltage setting block. In CCD systems a 5k part is installed here to give +/- 10 volts range to the outputs, whereas IR systems typically have larger values to limit the maximum voltage range to lower values. Typically a 10k resistor is installed for PICNIC or HAWAII arrays to set the range to 0 to +5 volts.

The addressing jumper block is also shown in Fig. 3. The four DAC jumpers select one of sixteen clock driver board numbers that may be installed in a system, with each selection allowing 48 voltages to be set, two for each of the 24 clock drivers. The clock driver jumper setting can be the same setting as the video processing address because bits in the 24-bit serial word other than those used to write to the DACs are used to write to the video boards. In supported readout code the clock driver number is usually set to 2, usually with the designation CLK2 = $002000. The bit assignment of the DAC data word is described below. The remaining three Switch jumpers are described above.

Up to eight separate clock driver boards executing different clocking timing may be installed in a single system. Up to sixteen clock driver boards may be installed and have different clocking voltages, but if more than eight are installed then one or more of them must have the same clocking timing. The jumper in the middle of the jumper block that is not labeled is not used, and is implicitly the zero bit = SS12 that is used to select between the lower and upper clock driver banks as explained above.

WRITING TO THE DIGITAL-TO-ANALOG CONVERTERS (DACs)

The DACs are loaded with digital numbers that are generated by the synchronous serial interface (SSI) circuit of the timing board DSP and transmitted to each DAC by a serial data stream that is decoded by PAL U70 (Programmable Array Logic) on each clock driver board. The serial data is sent in 24-bit words, most significant bit first, at a speed of 4.17 Mbits/sec. The 24-bit data word is decoded by the clock driver board as follows -

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
B3	B2	B1	B0	D3	D2	D1	D0	A0	A1	M1	M0	V11	V10	V9	V8	V7	V6	V5	V4	V3	V2	V1	V0

Board Number — Address of one of 4 DACs in each package

DAC select

DAC voltage, video processor gain or MUX select — Mode - DAC, gain or MUX select

Fig. 4: Bit assignment of serial word trasnsmitted to the clock driver for updating DACs.

B3 - B0 Selects the board number that is to be written to. The clock driver and video processor boards have four jumpers headers labeled "DAC address" that need to match the bits in the serial word for the board to accept it. The jumpers are installed to set the bit to zero. Up to 32 clock driver and 32 video

processor boards can be addressed in a system.

D3 - D0 Selects the DAC package number to be written to. There are twelve DACs on the clock driver board that are selected by numbers D = 0 to 11, and four DACs on the video processor that are selected by numbers D = 12 to 15. Note that clock drivers and video processor boards can have the same board select number. The Mode bits below must be zero (M0=M1=0)to write to a DAC.

If D2 = D3 = 0 then the V bits will set the MUX address.

If D2 = D3 = 1 then the V bits set the video processor gain.

A0 - A1 There are four DAC circuits in each package, and these two bits simply select which of the four is to be written to.

M0 - M1 Mode bits to select between DAC writes, gain select on video processors and output multiplexer (MUX) select on the clock driver board.

M0 = M1 = 0 to write to a DAC

M0 = M1 = 1 to select a gain or a MUX according to bits D2 and D3.

V0 - V11 The 12-bit digital number written to the DACs to select its output voltage, if writing to a DAC. If the video processing gain is selected then V0 to V3 sets the gain of channel 0 and V4 to V7 of channel #1. If the MUX is selected then they select which of 24 clock driver circuits are connected to the diagnostic connector for examination with an oscilloscope.

PINOUTS

The pinout of the male DB-37 output connector is shown in the table below. The waveform files that are INCLUDED in the timing application files generally contain these definitions.

For switch state = jumpered address				For switch state = jumpered address + 1			
Pin #	Signal Name	Switch State Bit Number	DAC addr. (hex)	Pin #	Signal Name	Switch State Bit Number	DAC addr.
1	CLK0	1	0 and 1	13	CLK12	1	$18 and $19
2	CLK1	2	2 and 3	14	CLK13	2	$1a and $1b
3	CLK2	4	4 and 5	15	CLK14	4	$1c and $1d
4	CLK3	8	6 and 7	16	CLK15	8	$1e and $1f
5	CLK4	$10	8 and 9	17	CLK16	$10	$20 and $21
6	CLK5	$20	$a and $b	18	CLK17	$20	$22 and $23
7	CLK6	$40	$c and $d	19	CLK18	$40	$24 and $25
8	CLK7	$80	$e and $f	33	CLK19	$80	$26 and $27
9	CLK8	$100	$10 and $11	34	CLK20	$100	$28 and $29
10	CLK9	$200	$12 and $13	35	CLK21	$200	$2a and $2b
11	CLK10	$400	$14 and $15	36	CLK22	$400	$2c and $2d
12	CLK11	$800	$16 and $17	37	CLK23	$800	$2e and $2f

20 +12 volt power supply, regulated, several hundred milliamps output current

21 -12 volt power supply, regulated, several hundred milliamps output current

DSP SOFTWARE

Below are presented several DSP code segments taken from several different source code files that illustrate software for writing to the clock driver DACs and clocks. This code all executes from the timing board, and is found in files by the names of "timhdr.asm", "tim.asm", and waveform files such as EEV4280.waveforms.

First, in "timboot.asm" the address of the switch state register is initialized:

```
WRSS    EQU     $FF80           ; Address of clock and video processor switches
        MOVE    #WRSS,R6        ; Register based address for quick access
```

Next, in "tim.asm" the address where the waveform table is located is written to the address register R0 and the clocking routine is invoked. The clocking routine is also located in "tim.asm":

```
        MOVE    Y:PARALLEL,R0   ; Address of parallel clocking waveform table
        JSR     <CLOCK          ; Call the clocking subroutine

; Core subroutine for clocking out CCD charge
CLOCK   MOVE    Y:(R0)+,X0      ; # of waveform entries
        MOVE    Y:(R0)+,A       ; Start the pipeline
        DO      X0,CLK1          ; Repeat X0 times
        MOVE    A,X:(R6) Y:(R0)+,A ; Send out the waveform
CLK1
        MOVE    A,X:(R6)        ; Flush out the pipeline
        RTS                     ; Return from subroutine
```

The table of waveforms is generally located in a separate file, and contains mnemonics for generating the 24-bit words that will be written to the clock driver board by the CLOCK subroutine. This file is an INCLUDE file that is named at the very bottom of the "tim.asm" file.

```
CLK3    EQU     $003000     ; Clock driver board select = 3 = top bank of board #2
P_DELAY EQU     $B00000     ; Parallel clock delay
I1      EQU     1           ; Image, phase #1, Pin 13 of the clock driver board
I2      EQU     2           ; Image, phase #2, Pin 14
I3      EQU     4           ; Image, phase #3, Pin 15

; Clock the Parallel clocks : I1->I2->I3. Store charge under I3 when the routine exits.
PARALLEL DC     SERIAL-PARALLEL-2       ; Compute number of waveforms
        DC      CLK3+P_DELAY+00+00+I3   ;  Let only I3 be high
        DC      CLK3+P_DELAY+I1+00+I3   ; Share charge between I1 and I3
        DC      CLK3+P_DELAY+I1+00+00   ;  Move charge to just I1
        DC      CLK3+P_DELAY+I1+I2+00   ; Share charge between I1 and I2
        DC      CLK3+P_DELAY+00+I2+00   ; Move charge to just I2
```

```
            DC      CLK3+P_DELAY+00+I2+I3       ; Share charge between I2 and I3
            DC      CLK3+P_DELAY+00+00+I3       ; Move charge to just I3
SERIAL                                          ; Waveforms for serial clocking
```

The next step to operate the clock driver is to write the voltage numbers to the DAC. This is generally done in a power on or set bias subroutine included in the file "timCCDmisc.asm" located in the directory DSPlib. The program structure is much the same as the clocking sequence above:

```
            MOVE    #DACS,R0            ; Get the starting address of the DAC values
            JSR     <SET_DAC            ; Write the numbers to each DAC

; Core routine for writing voltage and offset values to the DACs
SET_DAC     MOVE    Y:(R0)+,X0          ; Get the number of table entries
            DO      X0,SET_L0           ; Repeat X0 times
            MOVEP   Y:(R0)+,X:SSITX     ; Send out the waveform
            JSR     <PAL_DLY            ; Wait for SSI and PAL to be empty
            NOP                         ; Do loop restriction
SET_L0
            RTS                         ; Return from subroutine
```

Next the waveform tables are set up. SSITX is an address in the DSP for transmitting over the synchronous serial interface port. The DACs for all 24 circuits are accessible with the board address. Each clock driver circuit has two numbers written to its associated DACs, the high and low voltage, that are encoded as voltages in the source code file as RG_HI and RG_LO in this example, and converted to 12-bit numbers by the @CVI assembler directive. The assumption is that this is a CCD clock driver with +10 and -10 volt maximum rails.

```
SSITX       EQU     $FFEF       ; SSI transmit Data reigster
CLK2        EQU     $002000     ; Clock driver board select = 2
RG_HI       EQU     2.0         ; Reset Gate High voltage
RG_LO       EQU     -5.0        ; Reset Gate Low voltage
DACS        DC      END_DACS-DACS-1
            DC      (CLK2<<8)+(0<<14)+@CVI((RG_HI+10.0)/20.0*4095) ; Pin #1 High
            DC      (CLK2<<8)+(1<<14)+@CVI((RG_LO+10.0)/20.0*4095); Pin #1, Low
END_DACS
```