ARC-42: Dual Channel Infrared Video Processor Board

The board serves two functions - processing and digitizing the video outputs from the IR focal plane array (FPA) and supplying DC bias voltages to the FPA. It contains two identical video processing circuits that simultaneously process and digitize signals from two FPA video outputs. Two 16-bit analog-to-digital (A/D) converters are provided on the board, each with a total sample and conversion time of one microsecond. Their digital outputs are multiplexed on the backplane and read by the ARC-22 timing board for transmission to the host computer. The DC bias supply section of the board provides six separate low-noise, digitally programmable voltages suitable for direct connection to FPAs, as well as a video offset voltage for each of the two video processors.

THEORY of OPERATION

The video input circuitry contains a three op amp differential amplifier circuit for each of the two video inputs to the board. It is populated with Analog Devices AD829 op amps, which have low overall voltage and current noise, and especially low noise at low frequencies. The two A/D converters, Datel ADS937 parts, have an input voltage range of 0 (0 ADU output) to -10 volts (64k ADU output). For IR arrays such as the HAWAII and PICNIC whose output voltages go lower for increasing illumination, it is appropriate to connect their video outputs to the non-inverting input so the image counts increase with increasing illumination. The default gain of the differential amplifier is x2, which is appropriate for operation with a preamplifier gain of about x5 with FPAs that have a voltage swing of around one half to one volt between dark and full well illumination. Alternatively, the inputs can be connected directly to the FPA source followers, in which case the gain would be set much higher. In this case the controller should be located close to the FPA and the video wiring should be shielded since they are susceptible to noise pickup because of the relatively high output impedances of typical FPAs. Other values of the gain can be installed at the factory on request or changed by the user by altering the feedback. The video signals are brought in on the 9-pin DB-9 male connector P1, whose pinout is shown in Table 1 below.

TABLE 1 – Input Video Connector (DB-9)

DB9 pin #	Function
1	Inverting video input, Channel A
2	Non-inverting video input, Channel A
3	Inverting video input, Channel B
4	Non-inverting video input, Channel B
5,6,7,8,9	Ground

There are two coaxial SMB (push-on) connectors, located on either side of the DB-9 video connector. These contain the amplified video signals connected to the A/D converters. These can be used to safely monitor the video signals with an oscilloscope.

The A/D converter samples its input for 300 nanoseconds before its start A/D signal goes

high, and requires another 700 nanoseconds before its digital output data are valid. The digital output data are written to a latch when the XFER signal is clocked high, and then transmitted over the backplane when the timing board asserts the appropriate A/D selection lines. These signals need to be updated every pixel, and are latched by the WRSS (write switch state) signal generated by the timing board.

TABLE 2 - Fast timing control bit definitions

Function	Name	Control bit	Description
Start A/D #A	AD-A	SS0	Low to high transition starts conversion
Transfer counts #B	XFER-A	SS1	Low to high transition latches A/D
counts Not used		SS2	
Not used		SS3	
Start A/D #B	AD-B	SS4	Low to high transition starts conversion
Transfer counts #B	XFER-B	SS5	Low to high transition latches A/D
Not used		SS11-6	

The 12-bit DACs for the DC bias supplies receive their digital data words over serial lines from the PAL U8. The PAL converts 24-bit words from the timing board's synchronous serial interface (SSI) to 16-bit serial words routed to each DAC. These 24-bit words are listed below in Table 3, where n denotes the DAC address of the board and xxx the 12 bits setting the DAC voltage.

Positive voltages are required for PICNIC and HAWAII FPAs, so both DACs are set for unipolar positive operation. The first two outputs are routed to an offset control that shifts the A/D counts around. A table of default settings follows, where names are assigned to the DC bias signals used to operate PICNIC or HAWAII FPAs.

TABLE 3 - DC bias voltages definitions for positive unipolar operation (DB-15)

DB15 pin #	Function	Voltage range	DAC addr.	Default Voltage	Description
None	OFFSET-A		$nC0xxx		A/D offset, ch. A
None	OFFSET-B		$nC4xxx		A/D offset, ch. B
1	VOFFSET	0 to +5	$nC8xxx	+3.70	Preamp offset
2	VRESET	0 to +5	$nCCxxx	+0.50	Reset
3	VD	0 to +5	$nD0xxx	+5.00	Analog power
4	ICLT	0 to +5	$nD4xxx	+3.70	Current control
5	VDD	0 to +5	$nD8xxx	+4.00	Digital power
6	Available	0 to +5	$nDCxxx		
9					+15 volts power
10					-15 volts power
11-15	Ground				

BOARD JUMPERING

The jumpers located beneath the PAL U6 in the upper right region are of the board select the address of the board used to write to the DACs, read the two A/D converters and operate the fast timing control bits, marked SWITCH on the board. The jumpers are binary weighted with a jumper installed being a zero. The least significant bits are marked "0" on the silk screen and located on the left of each group. The default software has the address for the control bits set to zero (all jumpers installed), and the DAC and A/D addresses always the same, increasing from zero upwards.

There is a group of jumper headers JP15-17 and JP19 that is used to select the polarity of the DC bias supplies and video offsets, done by choosing the appropriate reference voltages for the two DACs used to set these voltages. These can be set to either unipolar positive, unipolar negative or bipolar. The resistor R74 is used to set the maximum voltage output of the DC bias supplies, while the zener diodes D5 and D6 limit the output voltages from the reference circuits to safe values. Finally, a set of zener diodes in a socketed header D5 is used to limit the output voltages of the board before they exit the connector P2. All these jumpers, diodes and the resistor are selected based on the maximum voltage that a particular FPA requires. These are typically +3.3, +5.0 (for MCT material) and -7.5 volts (for InSB material).

There are four more jumper headers that merit brief mention. JP18 connects the analog ground plane to the digital ground plane. It is normally installed, but users may remove it to experiment with alternative grounding architectures. JP1 and JP14 are no longer used for anything. JP20 can be used to change the video offsets by large values if difficulty is encountered bringing the video signal within range of the A/D converters.