

ARIES Warm Preparations

WBS/subelement	Issue or Topic	Progress	Imminent steps
Controller/EEPROM	<p>No ability to program a blank EEPROM.</p> <p>Pisces/ARIES EEPROMs have failed or been given away. We've been using the last one now since 2018.</p> <p>EP-1 is a vintage programmer from 1980s that requires real DOS.</p>	<p>Reverse-engineered EP-1 to determine that XMODEM is the protocol and there is no proprietary header. Plain XMODEM transfers should work! EP-1 may be future-proof after all. [It is now. 3/10]</p> <p>Required docs:</p> <ul style="list-style-type: none"> Ep-1 manual and EP.EXE for serial-sniffing 	<p>Try to use minicom under MacOS/BSD/Linux to XMODEM a file to EEPROM and verify same contents from read back. [Tested under NetBSD and MacOS -- 3/10]</p> <p>Generate EEPROM from scratch, see that it fully works w/ SDSU controller. [DONE for GENIII, 3/10] [GENII needs testing - TO DO]</p> <p>Buy more blank EEPROMs. [FOUND MORE SPARES - 3/10]</p> <p>Document the process. [PARTIAL]</p>
Controller/EEPROM	<p>Standard EEPROM build process does not work for EP-1 burns. Needs to be SREC or similar format.</p> <p>Must be possible; we did this in 2004...</p>	<p>Using the SREC converter from Motorola does not generate the correct-looking code.</p> <p>It writes to EEPROM but doesn't actually work in the controller.</p> <p>Required docs:</p> <ul style="list-style-type: none"> 56x000 DSP compiler documentation Old IRL EEPROM burn files 	<p>Use known-good EEPROM burn file from GenII controller (2004 code) to understand format. [DONE 3/10]</p> <p>Alter build process on GenII code to replicate this file. Burn to EEPROM and verify it works on GenII as per above. [New build system under wine works, results not tested on GenII controller yet.]</p> <p>Now do the same for GenIII. [DONE and works! 3/10]</p> <p>Document the process. [PARTIAL]</p>

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Controller/Test Setup	Set up controlled test environment for benchtop test.		Safe ARIES, move controller harnesses to table in controlled configuration, Saleae and DVM, ESD protect, etc.

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Controller/Verification	Verify new code for legacy ARC-46 video board to trace all digital clock signals and analog voltages.	<p>Tested on one “quadrant” previously. Serial transfers were not tested.</p> <p>Required docs to proceed:</p> <ul style="list-style-type: none"> • ARIES wiring schematics • H2RG manual (2005) • Datasheet for LTC1608ACG • SDSU documentation for legacy ARC-46 (Oct 2003) • Schematics for legacy ARC-46 (Oct 2003) <p>Software/hardware required:</p> <ul style="list-style-type: none"> • Saleae analyzer • Initial testing can be done with SDSU/OWL to verify operation. 	<ol style="list-style-type: none"> 1. Use Saleae analyzer on each digital line to verify pixel and line clocks 2. Verify serial register communication and configuration matches documentation. 3. Verify analog biases for H2RG. 4. Test grounded inputs: <ol style="list-style-type: none"> a. Open controller and swap cards to get video board access. b. Probe hardware inputs and outputs to ADC; adjustments needed to be in range? c. Software: adjust DACs, achieve observe working readout. Verify stable output and noise level. 5. Look up what analog output is expected from H2RG. Set up 4-way voltage divider on breadboard to put different signals on each “quadrant” to simulate a real array. Repeat the tests of step #3. Also verify de-interlacing using SDSU interface. 6. Document results. Documented success means we move to cold testing.

WBS/subelement	Issue or Topic	Progress	Imminent steps
Controller/Verification	Verify new code for CLIO ARC-46 rev3a video board to trace all digital clock signals and analog voltages.	<p>Replicated NIRCAM test code with ARIES wiring configuration. Semi-tested in lab configuration. Probably some bugs left...</p> <p>Required docs:</p> <ul style="list-style-type: none"> • ARIES wiring schematics • H2RG manual (2005) • Datasheet for AD7641LQFP • SDSU documentation for new ARC-46 (July 2011) • Schematics for rev3A ARC-46 (May 2007) <p>Software/hardware required:</p> <ul style="list-style-type: none"> • Saleae analyzer • Initial testing can be done with SDSU/OWL to verify operation. • Validate NIRCAM 56300 microcode with all of the pertinent changes to match the ARIES configuration. • Need to scrounge Dsub connectors of the appropriate gender and pin count for interfacing new video board. Easy Digikey order otherwise. 	<ol style="list-style-type: none"> 1. Replace point-to-point “ball of wires” testing harness with Dsub-terminated harness. 2. Use Saleae analyzer on each digital line to verify pixel and line clocks. 3. Verify serial register communication & configuration matches documentation. 4. Verify analog biases for H2RG. 5. Test grounded inputs: <ol style="list-style-type: none"> a. Open controller and swap cards to get video board access. b. Probe hardware inputs and outputs to ADC; adjustments needed to be in range? c. Software: adjust DACs, achieve observe working readout. Verify stable output and noise level. 6. Look up what analog output is expected from H2RG. Set up 4-way voltage divider on breadboard to put different signals on each “quadrant” to simulate a real array. Repeat the tests of step #3. Also verify de-interlacing using SDSU interface. 7. Document results. Documented success means we move to cold testing.

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Instrument/Software	<p>Add H2RG support to ARIES backend code.</p> <p>(Can be deferred to after cold tests.)</p>	<p>Two main trades:</p> <ol style="list-style-type: none"> 1. Update ARIES infrastructure to use "device-independent" v3.5 SDSU APIs 2. Add H2RG support to existing "LiL" (Leach in Linux) interface. 	<p>Option 1 should be evaluated against Pisces first.</p> <p>Option 2 needs bug-fixes merged from SDSU into LiL.</p> <p>Prototype, decide, implement, test against initial test results using OWL and the SDSU v3.5 API.</p>
Instrument/Software	<p>Plumb more generalized support into ARIES GUI and data system.</p> <p>(Can be deferred to after cold tests.)</p>	<p>Not started.</p> <p>Expectation is to further the existing MacOS,IOS app with compatibility with GNUstep on Linux.</p> <p>Alternates are:</p> <ul style="list-style-type: none"> • PyQT interface • Web browser interface 	<p>Initial design, including housekeeping, calibration, remote operations, and other desirables.</p> <p>Merge bug-fixes and other wants/needs from last "TO DO" list into this development effort.</p>
Instrument/Documentation	<p>Merge test reports and existing documentation onto wiki</p>	<p>Old wiki died with 2004 aries computer. Wiki data and instrument data were archived. Science data are available by ssh to soral.as.arizona.edu and a mediawiki instance is ready to accept the aries wiki data.</p>	<p>Merge aries wiki data into mediawiki on soral.</p> <p>Wiki is observer-centric. Add categories for test data and instrument documentation.</p>