| **WBS/subelement** | **Issue or Topic** | **Progress** | **Imminent steps** |
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| **555/Sunpower AVC** | 0C cold start failure in TVAC of STO-2 prototype controller | ~~Have RMA, working a quote with Sunpower regarding engineering time to understand the issue and determine if it also applies to potential flight units.~~Determined that power module is fried and these early rev boards “do that”. Best bet is to buy another: see writeup and updates to costs. | Best path is likely to:* Return unit w/ contract to evaluate DONE, no contract needed
* Upon return w/test report, redo TVAC test. Need new unit.
* Ideal: ability to recover from controller faults (reflash, etc)
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| **555/Sunpower AVC** | RFQ update for flight units | Seven-point update to quote issued:1. Vacuum compatible AVC
2. Performance screening of CTs
3. Reduce number of COTS harnesses
4. Add solder terminal PCB for CT
5. Replace 90-degree water jacket terminations w/ straight-out
6. Verify pressure vessel cooling jacket
7. Replace all compression fittings with VCR
 | Cliff is updating…price will go up, at $80K and climbing.See Sunpower discussion, current best options are $87K and $98K.Vacuum-compatible accelerometer PCB option (need to discuss; it’s expensive, >$10K upper)Need date at Ball is coming up!Need to start PO right after KDP-C confirmation. |
| **555/CPUB** | microSD card, on Critical Item List (CIL)Assemble sample list for testing | Samsung EVO+Samsung PROSanDisk ExtremeSanDisk Extreme PlusSanDisk IndustrialATP IndustrialTranscend IndustrialSwissbits SLC (S-450)Swissbits pSLC (S-46)Swissbits MLC (S-45) | Purchase remaining test items not self-bought or left-over from HEAT.DONEDetail downselect process to 2 models (primary, secondary).Batch-purchase the flight units after KDP-C.  |
| **555/CPUB/FSW** | microSD card (on CIL)Detail testing plan to:1. Detect counterfeits
2. Evaluate basic performance and reliability at room temp
3. Enhanced testing: loss of power tests, extended writes
4. Thermal/vac test plan
 | Evaluated known failures from prior testing and use on STO-2 and HEAT.1. Visual inspection, hardware writes to capacity, performance testing
2. Basic OS install and benchmark for throughput, latency, errors (dd, md5, unixbench, bonnie, iozone)
3. Power cycling test (full day)
4. Repeat limited tests from #2 and #3 in TVAC through thermal cycle
 | Construct hardware and software testing infrastructure and documentation of tests.microSD card TVAC testing in sequence with standard CPUB tests |
| **555/CPUB/FSW** | SPI, GPIO userspace driver on both Linux and NetBSD needs work:1. Linux interface shipped by vendor already deprecated in mainline
2. NetBSD needs to expose SPI speed & mode to userspace
 | From issues at left:1. Using Linux implementation as-is for now.

ISSUE: SPI bus CS improperly driven. Direct drive from TS4900 works but SPI test board is erratic.1. Wrote NetBSD kernel patch to expose more of the SPI interface to userspace, as we do with I2C. Mode and speed setting: ioctl, but per-transaction (no sessions)
 | 1. Continue evaluation of HKB and CPUB using Linux SPI implementation.

(currently fixing desktop SPI)1. Test BSD implementation on RPI3 (known SPI platform) using evaluation boards
2. Migrate SPI implementation to the TS-4900 port and test.
3. Merge changes upstream to CURRENT

This is foundational to most of the GUSTO FSW. |
| **555/CPUB/FSW** | uBoot programming to allow failover capability from microSD(X/H)C to eMMCThis is a key mitigation for a SEU that prohibits booting from one device | Developed basic uBoot implementation. Issues: 1. Can eMMC support GUSTO operations?
2. Can NetBSD live on the eMMC?
3. Does failover really work in real life? Net improvement in reliability?
 | Answers to evaluate:1. If we standardize on a very minimal root FS, yes. Otherwise microSD will be more capable.
2. Should be no issue… but yet to be tried
3. Requires a testing plan
 |
| **555/CPUB/FSW** | USB flash storage,Selection and testingData computer only | All units are commercial MLC, extended temp, -25C to 85CSanDisk Cruzer 64GB nominal.Testing process identical to microSD.Device failure must not screw up boot process. Mounting of device done manually or long after system start, to allow remote login / disabling device. | Need to purchase test models for evaluation and DPA.Construct hardware and software testing infrastructure and documentation of tests. |
| **555/CPUB/FSW** | SSD selection and testingData computer only | Intel SSD D3 S4610 1 TB is expected flight device. Prior model, DC S3500 is obsolete. Good news is the cost went down by x3! Testing process identical to microSD.Device failure must not screw up boot process. Mounting of device done manually or after system start, to allow remote login / disabling. | Purchase for initial testing and TVAC. This will be the DPA unit. If OK, buy 2 more as flight units around CDR.Note that this is nominally a 0-70C device! Needs evaluation outside of normal environmental spec. May need heater. |
| **555/CPUB/FSW** | RS-422 and RS-232 port evaluation | Developed basic test plan:Control MDrive motor from HEAT using RS-422 interfaceControl 2nd gen Cryotel CT controller (from HEAT) using RS-232 | Need to develop the testing cabling and harnesses and actually do the end-to-end test.Document, add hkServer & opticsServer callbacks, merge into git, merge into ATF. Add to EM testbed. |
| **555/CPUB/FSW** | Need to add gondola style EPS-8100 network switch to testbed | Purchased.  | Need to crimp RJ45 to Molex connectors and apply to STO-2 testbed for initial tests, then TVAC with CPU board. |
| **555/HKB/FSW** | AD590 and mux | Seems to work wellAlso seems to fall under the same erratic SPI issues when Saleae probes are removed.  | Fix SPI bus.Test with CPUB, not TS-8550.Noise, precision, calibration measurements (per L4 reqmts)Document, add hkServer callbacks, merge into git, merge into ATF and EM testbed. |
| **555/HKB/FSW** | DT670 silicon diodes and mux | Not getting sensible values from diodes, not seeing a change in diode channel. Seems to be the SPI bus drive impedance.  | Fix SPI bus. Debug with hardware and software probes/breakpoints to evaluate. Test again with CPUB. |
| **555/HKB/FSW** | Helium flowmeter | Need to integrate with STO-2 model and test. Can simulate with an external voltage. | Develop and execute test.Document, add hkServer callbacks, merge into git and ATFThe STO-2 flowmeter is not available. GM50A is new model. Should purchase unit to evaluate changes and verify. |
| **555/HKB/FSW** | Helium level sense | Have not attempted to operate… | Develop and execute crude test with variable external resistor.Can we enable and disable the sensing circuit?Verify 75 mA current source and record time series of resistance measurements.Document, add cryoServer callbacks, merge into ATF |
| **555/HKB/FSW** | Further Safety Critical software development | Process identified in SDP/SAPGUSTO-UA-DOC-00019 | Need to sketch how this is going to work in CryoServer. |
| **555/FSW** | Git, Bitbucket, and Jira workflows | Stalled for now. Need to be fully in process well before peer review.Good starting point would be the initial merge of FSW to the git tree. | Migrate soral to FreeBSD 12 to support GUSTO thru life cycleMigrate Jira and Bitbucket to 8.x for GUSTO life cycleDevelop simple workflow and move current work items into ticketsMigrate working GUSTO code into git and start using it for everything. |
| **555/FSW** | Socket server architectural changes to serve error handling needs | * Polling vs event-driven
* Syntactical handling of command options without garbling code
* How to pass errors upstream when no unsolicited messages are allowed:
	+ Housekeeping packet
	+ Watchdog process
 | Evaluating simplest path forward; polling with exceptions. |
| **555/FSW** | DAC code review/audit | Need to perform. | Identify path forward. Work toward increased modularity and code clarity |
| **555/FSW** | Omnisys software ICD readback | Received from Omnisys Evaluating, collecting comments | Respond to Omnisys with accumulated comments, set up working group to discuss |
| **555/PID power supplies** | Current CAD for PID power supplies is too large, too much power dissipation, too far away from the LOsNeed verification by test that biasing Vtune on DC/DC modules is safe | Developed schematic, purchased parts to test a PID power supply based on TPS5430-EP and SPI-driven digipots.More efficient than PTN78020W from HEAT and STO-2.PTN78060W is a backup for prototyping.Parts arrived late last week for breadboarding. | Breadboard a test, demonstrate PID output voltage adjustability. DONEOperate a PID output at 5, 20, 60, and 600 Hz and evaluate output.If successful, make baseline and merge results into PEL.TVAC and move onto detailed design and layout. |
| **555/Band 1-2 LO controllers/FSW** | Need to get to a preliminary design. | Schematic on SOEDMS for reviewAsked VDI to verify the changes to voltages and bypass resistor. | Evaluate schematic for layout and design overall controller software concept.Looking for simplifications to reduce part count.However, may need to add high-side switches for button heaters?Merge design changes back to Electronics document (-00034) and VDI ICD (-00049).  |
| **555/Band 3 LO controllers/FSW** | Need to get to a preliminary design. | Feeling neglected | Evaluate PDR green-block diagram and ancillary COTS parts. Is it still accurate?  |
| **730/GSW** | Python-based DRM has no formal power-system awareness. Some scenarios work scientifically but may not be schedulable. | PDR-level product is probably inconsistent with Pietro’s power system CONOPS at some level.Needs refinement for CDR.Observing Table is generated but no closed-loop validation except by explicitly running through ACE. | Start CONOPS working group.Basic power calculations to be added to DRM with feedback from PietroDRM will be released and go under configuration managementUse this to answer MPDR RFA#8. Pietro to replace with his analysis or accept. |

**ARIES Warm Preparations**

| **WBS/subelement** | **Issue or Topic** | **Progress** | **Imminent steps** |
| --- | --- | --- | --- |
| **Controller/EEPROM** | No ability to program a blank EEPROM. Pisces/ARIES EEPROMs have failed or been given away. We’ve been using the last one now since 2018.EP-1 is a vintage programmer from 1980s that requires real DOS.  | Reverse-engineered EP-1 to determine that XMODEM is the protocol and there is no proprietary header. Plain XMODEM transfers should work! EP-1 may be future-proof after all. [It is now. 3/10]Required docs:* Ep-1 manual and EP.EXE for serial-sniffing
 | Try to use minicom under MacOS/BSD/Linux to XMODEM a file to EEPROM and verify same contents from read back. [Tested under NetBSD and MacOS -- 3/10]Generate EEPROM from scratch, see that it fully works w/ SDSU controller. [DONE for GENIII, 3/10] [GENII needs testing – TO DO]Buy more blank EEPROMs. [FOUND MORE SPARES - 3/10]Document the process. [PARTIAL] |
| **Controller/EEPROM** | Standard EEPROM build process does not work for EP-1 burns. Needs to be SREC or similar format.Must be possible; we did this in 2004… | Using the SREC converter from Motorola does not generate the correct-looking code. It writes to EEPROM but doesn’t actually work in the controller.Required docs:* 56x000 DSP complier documentation
* Old IRL EEPROM burn files
 | Use known-good EEPROM burn file from GenII controller (2004 code) to understand format. [DONE 3/10]Alter build process on GenII code to replicate this file. Burn to EEPROM and verify it works on GenII as per above. [New build system under wine works, results not tested on GenII controller yet.]Now do the same for GenIII. [DONE and works! 3/10]Document the process. [PARTIAL] |
| **Controller/Test Setup** | Set up controlled test environment for benchtop test. |  | Safe ARIES, move controller harnesses to table in controlled configuration, Saleae and DVM, ESD protect, etc. |
| **Controller/Verification** | Verify new code for legacy ARC-46 video board to trace all digital clock signals and analog voltages. | Tested on one “quadrant” previously. Serial transfers were not tested.Required docs to proceed:* ARIES wiring schematics
* H2RG manual (2005)
* Datasheet for LTC1608ACG
* SDSU documentation for legacy ARC-46 (Oct 2003)
* Schematics for legacy ARC-46 (Oct 2003)

Software/hardware required:* Saleae analyzer
* Initial testing can be done with SDSU/OWL to verify operation.
 | 1. Use Saleae analyzer on each digital line to verify pixel and line clocks
2. Verify serial register communication and configuration matches documentation.
3. Verify analog biases for H2RG.
4. Test grounded inputs:
	1. Open controller and swap cards to get video board access.
	2. Probe hardware inputs and outputs to ADC; adjustments needed to be in range?
	3. Software: adjust DACs, achieve observe working readout. Verify stable output and noise level.
5. Look up what analog output is expected from H2RG. Set up 4-way voltage divider on breadboard to put different signals on each “quadrant” to simulate a real array. Repeat the tests of step #3. Also verify de-interlacing using SDSU interface.
6. Document results. Documented success means we move to cold testing.
 |
| **Controller/Verification** | Verify new code for CLIO ARC-46 rev3a video board to trace all digital clock signals and analog voltages. | Replicated NIRCAM test code with ARIES wiring configuration. Semi-tested in lab configuration. Probably some bugs left…Required docs:* ARIES wiring schematics
* H2RG manual (2005)
* Datasheet for AD7641LQFP
* SDSU documentation for new ARC-46 (July 2011)
* Schematics for rev3A ARC-46 (May 2007)

Software/hardware required:* Saleae analyzer
* Initial testing can be done with SDSU/OWL to verify operation.
* Validate NIRCAM 56300 microcode with all of the pertinent changes to match the ARIES configuration.
* Need to scrounge Dsub connectors of the appropriate gender and pin count for interfacing new video board. Easy Digikey order otherwise.
 | 1. Replace point-to-point “ball of wires” testing harness with Dsub-terminated harness.
2. Use Saleae analyzer on each digital line to verify pixel and line clocks.
3. Verify serial register communication & configuration matches documentation.
4. Verify analog biases for H2RG.
5. Test grounded inputs:
	1. Open controller and swap cards to get video board access.
	2. Probe hardware inputs and outputs to ADC; adjustments needed to be in range?
	3. Software: adjust DACs, achieve observe working readout. Verify stable output and noise level.
6. Look up what analog output is expected from H2RG. Set up 4-way voltage divider on breadboard to put different signals on each “quadrant” to simulate a real array. Repeat the tests of step #3. Also verify de-interlacing using SDSU interface.
7. Document results. Documented success means we move to cold testing.
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| **Instrument/Software** | Add H2RG support to ARIES backend code.(Can be deferred to after cold tests.) | Two main trades:1. Update ARIES infrastructure to use “device-independent” v3.5 SDSU APIs
2. Add H2RG support to existing “LiL” (Leach in Linux) interface.
 | Option 1 should be evaluated against Pisces first.Option 2 needs bug-fixes merged from SDSU into LiL. Prototype, decide, implement, test against initial test results using OWL and the SDSU v3.5 API. |
| **Instrument/Software** | Plumb more generalized support into ARIES GUI and data system.(Can be deferred to after cold tests.) | Not started. Expectation is to further the existing MacOS,IOS app with compatibility with GNUstep on Linux.Alternates are:* PyQT interface
* Web browser interface
 | Initial design, including housekeeping, calibration, remote operations, and other desireables. Merge bug-fixes and other wants/needs from last “TO DO” list into this development effort. |
| **Instrument/ Documentation** | Merge test reports and existing documentation onto wiki | Old wiki died with 2004 aries computer. Wiki data and instrument data were archived. Science data are available by ssh to soral.as.arizona.edu and a mediawiki instance is ready to accept the aries wiki data. | Merge aries wiki data into mediawiki on soral. Wiki is observer-centric. Add categories for test data and instrument documentation.  |